Remarks

In the Office Action, claims 1-6, 16-19, 32 & 34 were rejected under 35 U.S.C. 102(e) as being anticipated by Greenfield et al. (U.S. Patent No. 5,760,836), while claims 7-15, 20-31, 33 and 35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al. further in view of Choe et al. (U.S. Patent No. 6,094,696). Applicants respectfully, but most strenuously, traverse these rejections and request reconsideration. Claims 1-35 remain pending.

As is well known, there is no anticipation of a claim unless (1) all the same elements are (2) found in exactly the same situation and (3) are united in the same way to (4) perform the identical function. In this case, the encoding techniques of Greenfield et al. clearly do not have the same elements, nor are they capable of being readily modified to include the same elements, as that recited by applicants in independent claims 1 & 16.

Applicants recite in these independent claims a technique for encoding a digital video image stream in an encoder. The technique includes feeding back to hardware logic within the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read, and counting therefrom the number of bits read by a host (R). The technique further includes determining the number of bits encoded and written into an external buffer (E), and in hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF). The technique further includes providing, from the hardware logic of the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

Dependent claims 32-35 further recite that the continuous updating comprises obtaining the fullness of the external buffer (BF) every cycle of the encoder.

To restate, the present invention employs hardware to continuously monitor the real time fullness of the external buffer and provide a dynamic buffer level indicator indicative of the fullness of the external buffer. This dynamic buffer level indicator assists the host's application

and the control of reading compressed data from the external buffer coupled to the encoder. The buffer level indicator is dynamic in that the indicator is adjusted based on continuous monitoring of the external buffer, e.g., every cycle of the encoder. (See page 4, lines 26-33).

In support of the anticipation rejection, the Office Action alleges the teachings at columns 5-7 of Greenfield et al. disclose the above-summarized aspects of applicants' invention. This characterization of the teachings of Greenfield et al. is respectfully traversed. In support of this traversal and the following comments, applicants wish to note the significant overlapping in inventorship between the present application and the inventors of the Greenfield et al. patent. The enclosed Declaration by co-inventor Agnes Y. Ngai is provided to support applicants' characterization of the teachings and capabilities of the system described in Greenfield et al., and in support of the differences discussed hereinbelow with respect to that system. Agnes Y. Ngai is also a co-inventor on the Greenfield et al. patent.

Applicants respectfully submit that a careful reading of Greenfield et al. fails to uncover any teaching, suggestion or implication that the processing or logic described therein comprises a dynamic buffer level indicator that is provided as recited by applicants herein. In fact, Greenfield et al. specifically describes a non-continuous buffer level indicator as established by the Ngai Declaration. In Greenfield et al. the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield et al. would be incapable of supporting a continuously obtaining application as recited herein. Column 6, lines 18-29 specifically state that the microcode reads the register and compares it with the buffer fullness in bytes (BF/8). This means that the processor is doing the updating of the buffer level indicator and that the buffer level signal is not returned on a continuous basis. As one example, in the Greenfield et al. system, a buffer level indicator would be returned approximately once per macroblock or per frame. In contrast, applicants' hardware logic continuously obtains the fullness of the external buffer. In claims 32-35 this continuous obtaining is recited to occur with every cycle of the encoder, which is clearly incapable with a system such as described by Greenfield et al.

As noted at page 14 & 15 of applicants' specification, the disadvantage of the above-summarized approach (i.e., the Greenfield et al. approach) is that it is implemented in microcode, and therefore, buffer fullness in not constantly monitored. Without a continuous view of the fullness of the buffer, the host processor must wait until the microcode goes in, polls the on-chip register and calculates the fullness of the FIFO. This creates a latency issue which produces an inherent inaccuracy in the FIFO fullness reading.

The present invention solves this problem by implementing FIFO monitoring and a dynamic FIFO buffer level indicator in hardware logic inside the digital video encoder for interfacing, for example, to an industry standard FIFO buffer or cascaded FIFO buffers. Thus, applicants continuously attain the recited dynamic buffer level indicator through the use of a hardware implementation. Clearly, Greenfield et al. describes a microcode implementation, which, based on the processing described therein, comprises a non-continuous implementation. This is understood by one skilled in the art through the use of a non-real time counter to monitor the amount of data written to the FIFOs in Greenfield et al. (see column 6, lines 10- 11), and through the use of a non-continuous sampling of this counter by the microcode.

Responsive to the Examiner's comments contained in paragraph 5 at pages 6-9 of the final Office Action, applicants note that column 1, lines 37-49, column 5, lines 24-30 & 53-67, and columns 6 & 7 all discuss a real time encoder. However, these columns do not teach, suggest or imply continuous monitoring of external buffer fullness as recited in the independent claims presented herewith. Real time encoding is different from and independent of applicants' recited continuous monitoring of external buffer fullness.

In paragraph 5 of the final Office Action, the Examiner alleges that because Greenfield et al. describes real-time encoding, all components/processings within the encoder must inherently be performed in real-time as well. This conclusion is respectfully traversed, as supported by the Ngai Declaration submitted herewith setting forth the limitations of the Greenfield et al. software approach.

The doctrine of inherency is well-settled in patent law, and is best described in an excerpt from Hansgirg v. Kemmer, 26 C.C.P.A. 937, 102 F.2d 212, 40 U.S.P.Q. 665 (1939):

> Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. [citations omitted.] If, however, the disclosure [of the cited reference] is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient [to anticipate the claimed invention].

Id. at 940, 102 F.2d at 214, 40 U.S.P.Q. at 667; Stoller v. Ford Motor Co., 18 U.S.P.Q. 2d 1545, 1547 (Fed. Cir. 1991); Tyler Refrigeration v. Kysor Industrial Corporation, 227 U.S.P.Q. 845, 847 (Fed. Cir. 1985); Ex parte Levy, 17 U.S.P.Q. 2d 1461, 1464 (B.P.A.I. 1990); In re Oelrich and Divigard, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981).

In Ex parte Levy, the court stated that "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." Ex parte Levy, 17 U.S.P.Q. 2d at 1464 (lengthy citation omitted) (italics added). As clearly established by the Ngai Declaration, the Greenfield et al. system is incapable of continuously obtaining the fullness of the external buffer, let alone of obtaining the fullness of the external buffer every cycle of the encoder. Based upon this Declaration, applicants respectfully traverse the Office Action's stated position of inherency of the claimed subject matter within Greenfield et al., and reconsideration thereof is requested.

As noted above, the monitoring of external buffer fullness in Greenfield et al. is necessarily non-continuous based upon the teachings set forth therein. **In fact, the present invention arose from applicants' identifying of the deficiency of the Greenfield et al. teachings in this respect.** The formulas set forth in Greenfield et al. clearly indicate to one skilled in the art that the processor determination of buffer level fullness described therein is a non-continuous calculation. To further recite the difference, applicants point to claims 32-35 wherein the continuously obtained fullness of the external buffer is determined every cycle of the

encoder, i.e., every machine cycle. This is distinct from any teaching, suggestion or implication in Greenfield et al.

In view of the above, applicants respectfully submit that there are clear differences between the encoding technique recited in claims 1 & 16 and the teachings, suggestions or implications in Greenfield et al. Therefore, applicants request withdrawal of the anticipation rejection and allowance of independent claims 1 & 16, as well as the claims which depend therefrom.

As noted, claims 7-15, 20-31, 33 & 35 were rejected under 35 U.S.C. 103(e) as being unpatentable over Greenfield et al. further in view of Choe et al. This rejection is respectfully traversed.

An "obviousness" determination requires an evaluation of whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art. In evaluating claimed subject matter as a whole, the Federal Circuit has expressly mandated that functional claim language be considered in evaluating a claim relative to the prior art. Applicants' respectfully submit that the application of these standards to the independent claims presented herewith leads to the conclusion that the recited subject matter would not have been obvious to one of ordinary skill in the art based on the applied patents.

Assuming, arguendo, that the combination is proper, the combination fails to teach or suggest certain features of the claimed invention. For example, each independent claim at issue (i.e., claims 9 & 27) recites a technique wherein hardware logic within the encoder continuously obtains and provides to the host a dynamically updated flag. Neither Greenfield et al. nor Choe et al. continuously obtain and provide from encoder hardware to a host a dynamically updated flag. In fact, applicants note that Choe et al. does not even involve an encoding process.

As noted above, a careful reading of Greenfield et al. fails to uncover any teaching, suggestion or implication of hardware logic implementing a technique wherein a dynamic buffer

level indicator is continuously obtained and provided to a host. Similarly, a careful reading of Choe et al. fails to uncover any discussion of an encode process, let alone the provision of a dynamic buffer level indicator from an encoder to a host. In fact, a careful reading of Choe et al. fails to uncover any dynamic indicator being continuously provided, as disclosed in the present application. Choe et al. disclose a data transfer mechanism where a set of buffer_full and buffer_empty flags are implemented for each device. Once a flag is set it has to be reset by the CPU. This is in contrast with the flags disclosed by applicants which are dynamic, real time indicators. As the data is added to the pre-defined full level the buffer_full flag is asserted in applicants' case. Further as data is removed to below the pre-defined full level, the buffer_full flag is deasserted without any CPU intervention. The flags of Choe et al. are used to start data transfer operations. In contrast, the flags recited by applicants do not necessarily initiate data transfer. Applicants flags are used to regulate the data rate in and out of the FIFOs in a simultaneous and continuous manner.

For all the above reasons, applicants respectfully submit that independent claims 9 & 27 would not have been obvious to one of ordinary skill in the art based upon Greenfield et al. and Choe et al. In applicants' recited invention, hardware logic within the encoder performs certain functions, including subtracting from a number of bits encoded the number of bits read by the host to continuously obtain the fullness of an external buffer. Further, from this hardware logic, a dynamically updated flag is provided in real time to a host. Since applicants' invention is implemented within hardware logic within the encoder, no CPU intervention is required. In fact, only with a hardware implementation is it possible to obtain applicants' recited continuously obtaining the fullness of the external buffer and providing in real time the dynamically updated flag.

The dependent claims are believed allowable for the same reasons as the independent claims, as well as for their own additional characterizations. For example, claims 33 & 35 recite that the hardware logic continuously obtains the fullness of the external buffer every cycle of the encoder. A careful reading of the applied art fails to uncover any suggestion or capability that the systems described therein could obtain every cycle of the encoder the fullness of the external

buffer. In fact, this is simply not possible using a CPU based system such as described by Greenfield et al. and Choe et al.

In view of the above Amendments and Remarks, applicants respectfully request allowance of all claims pending herein. Should the Examiner wish to discuss the case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,

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